Protograph QC-LDPC Codes Design for Multi-Level Cell Flash Memories

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***Abstract*—In this letter, protograph based quasi-cyclic (QC) low-density parity-check (LDPC) codes are designed for multi-level cell (MLC) NAND flash memories, where the exact voltage signal values are unavailable but rather the quantized voltage signals are measured for soft decoding. Existing LDPC codes optimized for symmetric, additive white Gaussian noise (AWGN)-like channels are not optimal for flash memory channels due to their asymmetries. The proposed approach exploits the mutual information (MI) between input and output of flash memory to model the quantized log-likelihood ratio (LLR) messages. The proposed protograph based codes, whose base matrix is constructed according to the degree sequences optimized by the modified extrinsic information transfer (EXIT) chart method for NAND flash memories, have a low-complexity QC encoder structure with a readily parallelizable protograph decoder structure. Moreover, a rate-compatible family of protograph LDPC codes can be conveniently generated according to the proposed nested photograph. Simulation results and theoretical analyses are provided to support the advantages of the proposed coding scheme.**

***Index Terms*—protograph low-density parity-check (LDPC) codes, extrinsic information transfer (EXIT) chart, NAND flash, Multi-level cell (MLC).**

I. INTRODUCTION

High–density NAND flash memories by using multi-level cell (MLC) or triple-level cell (TLC) technique, which store 2 or 3 logical bits in a physical single memory cell, have recently been extensively researched to pursue higher storage capacity [1]-[2]. The low bit cost and high reliability are the most important requirements for NAND flash memories. Unfortunately, the reliability and performance of a NAND flash memory are largely destroyed due to scaling down the feature size of NAND flash cells and the related noise sources, such as the random telegraph noise (RTN), read/program disturb, retention noise (RN), and cell-to-cell interference (CCI) [3]-[4].

Due to the aggressive technology scaling and MLC technique, low-density parity-check (LDPC) code that is well-known for its capacity-approaching ability in the AWGN channel is believed to be indispensable for MLC NAND flash memories as well. LDPC codes with soft-decision decoding have been proposed as error correction codes (ECC) to solve the reliability issues of NAND Flash memory recently [5]-[6]. Results in [7] suggest that the best LDPC degree distributions are different for decoding scenarios with different levels of precision during multiple reads. Moreover, flash memory channels possess a significant amount of asymmetry. LDPC codes optimized for symmetric, AWGN-like channels have been used for Flash applications, not considering the error characteristics of flash memories. To help address this needs, the reciprocal channel approximation (RCA) based extrinsic information transfer (EXIT) function analysis is used to optimize the LDPC degree distributions and the word-line voltage in light of the multiple decoding attempts in [8]. However, the correspongding computational complexity is still huge compared with EXIT chart due to the fact that it's an approximation of the Density evolution (DE) algorithm. Based on new combinatorial definitions and linear algebraic tools, authors in [9] propose a theoretical framework for the design and analysis of non-binary LDPC (NB-LDPC) codes over data storage channels with asymmetry, which manipulates the edge weights in the graph representation of NB-LDPC codes.

A main challenge in the design of LDPC codes for flash memory channels is to describe the quanzited message in closed form since the output extrinsic log-likelihood ratio (LLR) messages from the flash channel cannot be approximated as a Gaussian distribution, when the common EXIT chart approach is employed. In [10], LDPC codes optimized for two-dimensional intersymbol interference (2D-ISI) channels have been designed, and are shown to achieve better performance than LDPC optimized for AWGN channels. An LDPC code degree distribution designed for a full-precision Gaussian channel may also not be optimal in the quantized setting. This motivates us to investigate the low-complexity optimization approach to design LDPC codes for the quantized flash memory channels.

In this letter, we design protograph based quasi-cyclic (QC) LDPC codes which are well-suited for MLC flash memories, exploiting the mutual-information between input and output of flash memory to model the quanzited LLR messages. The base matrix is constructed according to the degree sequences for the specific flash channels with modification to match the desired code rate and code length. The proposed protograph based codes have a low-complexity QC encoder structure with a readily parallelizable protograph decoder structure.

The rest of this letter is organized as follows. Section II introduces the MLC NAND flash channel model. Then in Section III, protograph based QC-LDPC codes are proposed for

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the MLC NAND flash channels and the normalized logarithmic asymptotic weight distributions are also computed. The proposed schemes are validated in Section IV. Finally, Section V presents the conclusions.

II. CHANNEL MODEL

MLC technique, storing two bits in a single memory transistor, allows the storage of twice as much data in the same area as the single level cell (SLC). The charges need be accurately placed to one of four charge states which is associated with a two-bit data pattern. A flash memory cell must be erased before data can be written by removing the charges in the floating gate, which sets its threshold voltage to the lowest voltage window. In this work, we adopt a simplified channel model for MLC NAND flash memories, as the proposed LDPC code design approach is generic and can be applied to other flash memory channel models as well.

Due to inevitable process variability, it has been observed that the threshold voltage of the erased memory cells tends to have a wide Gaussian-like distribution [11]. Following the MLC flash memory modelling in [11], we also assume other three cell threshold voltages follow Gaussian distributions as illustrated in equation (1), where μ_{XX} and δ_{XX} are the mean and standard deviation of the cell threshold voltage. The right subscript $_{XX}$ in mean and standard deviation stands for a two-bit data pattern with Gray mapping (see Fig.1). In this work, the relationship of the standard deviations is shown in equation (2). The locations of the means of the two inner distributions are determined to minimize the raw bit error rate (BER). The maximum voltage difference between the means of the two outer distributions is defined by $v_{\max} = \mu_{01} - \mu_{11}$. Fig.1 show the threshold voltage probability distribution of MLC NAND flash memory channel, where $\mu_{11} = 0$, $\mu_{10} = 3.25$, $\mu_{00} = 4.55$, $\mu_{01} = 6.5$, and $\delta_{00} = \delta_{10} = 0.28$, $\delta_{01} = 0.56$, $\delta_{11} = 1.12$.

$$p_{XX}(x) = \frac{1}{\delta_{XX}\sqrt{2\pi}} e^{-\frac{(x-\mu_{XX})^2}{2\delta_{XX}^2}} \tag{1}$$

$$\delta_{11} = 2\delta_{01} = 4\delta_{10} = 4\delta_{00} = 4\delta \tag{2}$$

Because the sense-amp comparator provides at most one bit of information about the threshold voltage, decoders for ECC in flash memory read the same sense-amp comparator multiple times with different word-line voltages to obtain the soft information. Typically in 4-level MLC flash memory, each cell is compared to 3 word-line voltages and thus the output of the comparator has 4 possible values (i.e., four distinct quantization regions). We extend the quantization approach in [7] which maximizes the mutual information (MI) between the input and output of a QPSK read channel to a more realistic MLC channel model described above. The maximum mutual information (MMI) based quantized channel signal is used in the LDPC code design in the next section.

III. PROTOGRAPH BASED CODE DESIGN

In this paper, we focus on the protograph based LDPC code design for MLC flash memory channels. We define V_{max} and C_max as the maximum variable node degree and maximum check node degree, respectively. Let $\boldsymbol{\lambda} = (\lambda_2, \lambda_3, \cdots, \lambda_{V_{max}})$ and $\boldsymbol{\rho} = (\rho_2, \rho_3, \cdots, \rho_{C_{max}})$ be the variable node degree sequence and check node degree sequence of a LDPC code, where λ_k or ρ_k is the fraction of edges connecting to a degree k variable or check node, respectively.

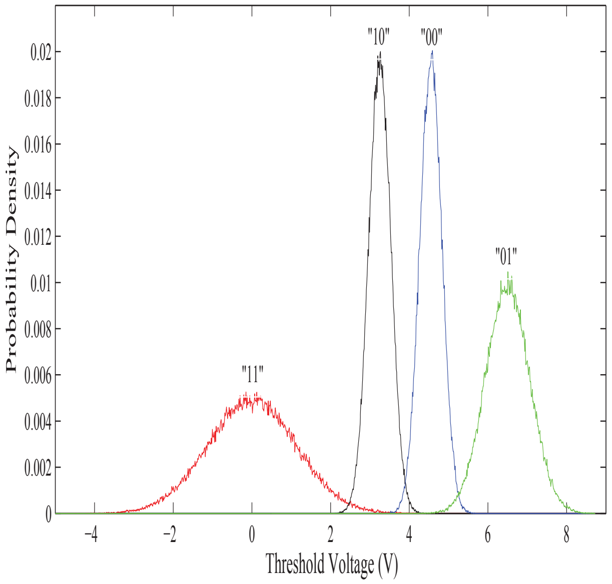

Fig. 1. Threshold voltage probability distribution of MLC flash memory.

A. Protograph Code Design for MLC Flash Memories

In MLC NAND flash memory channel, the reading signal is quantized, therefore the exact voltage signal value is unavailable but rather the quantized voltage signal is measured for soft decoding. These quantization levels can be designed by maximizing the MI between input and output of flash memory. One important assumption of employing the EXIT chart is that the output extrinsic LLR messages L_{ch} from the channel are approximately Gaussian distributed. Actually, we show that this assumption is not valid for the MLC NAND flash memory channel. Therefore the conventional EXIT chart method cannot be directly employed to flash memory channels. Unlike AWGN channel where the variance of L_{ch} conditioned on channel input X is easily computed, we cannot get a Gaussian-like distribution by using curve fitting. As shown in Fig.2, due to the nonlinearity of the quanziter, the LLR distributions of the channel output is no longer Gaussian, and the quanzited message L_{ch} cannot be described in closed form. By invoking the ergodicity theorem which states that expectation can be replaced by the time average, we measure the mutual information by a large number N of samples in Monte Carlo simulations for this unknown distributions. Therefore, we first track the quantized LLR distribution by $I_{(\xi,X)}$, which is measured by estimating the $p(\xi_{|x=0})$ and $p(\xi_{|x=1})$ from a histogram of the extrinsic information values, where ξ denotes the element of

LLRs. Given the $p(\xi_{|x=0})$ and $p(\xi_{|x=1})$, the mutual information of quantized channel is calculated by

$$I_{(\xi,X)} = \frac{1}{2}\int_{\xi}\sum_{x\in X} p(\xi_{|x})\log_2\left(\frac{2p(\xi_{|x})}{p(\xi_{|x=0})+p(\xi_{|x=1})}\right)d\xi \tag{3}$$

Then, the quantized LLR distribution is assumed to follow a Gaussian distribution with variance δ_{mlc}^2 from $I_{(\xi,X)}$, which is consistent with the fact that EXIT chart method tracking the extrinsic information by using a curve-fitting procedure is not sensitive to the actual LLR values.

The combined flash channel output signal and variable node detector (VND) EXIT function of a degree-d_v^i variable node is given by

$$I_{E,VND}^{d_v^i}(I_A, d_v^i, \xi) = J\left(\sqrt{(d_v^i - 1)[J^{-1}(I_A)]^2 + \delta_{mlc}^2}\right) \tag{4}$$

The optimized degree sequences of LDPC codes are designed by selecting the best $\boldsymbol{\lambda}$ sequence to make the combined EXIT curve of the quantized channel signal and VND fit the EXIT curve of the check node detector (CND) without crossing over, which is equivalent to solving the following linear programming problem

$$\min_{\lambda}\sum_{\kappa=1}^{N_\kappa}\left(\sum_{i=2}^{V_{max}}\lambda_i\times I_{E,VND}^{d_v^i}(\kappa) - I_{A,CND}(\kappa)\right)\times\delta_\kappa \tag{5}$$

subject to

$$\sum_{i=2}^{V_{max}}\lambda_i = 1(\lambda_i \geq 0)$$

$$I_{A,CND} \leq \sum_{i=1}^{V_{max}}\lambda_i\times I_{E,VND}^{d_v^i}$$

where N_κ is the total number of samples with interval δ_κ.

According to the degree sequences optimized by the modified EXIT chart method described above for the specific MLC NAND flash memory channel, we can design the base matrix of porotograph and the random-like photograph based LDPC code by using the progressive edge-growth (PEG) algorithm [10], which is further modified by imposing the additional QC constraints of the graph to construct the protograph based QC-LDPC codes. The procedure of protograph based QC-LDPC codes design is summarized in Algorithm 1.

Note that the mentioned LDPC code design method is not sensitive to the specific distribution of the channel modeling. Thus, the proposed approach can be easily extended to other flash memory channels.

Algorithm 1 Protograph based QC-LDPC design algorithm for MLC flash channel

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Initialize MLC flash channel parameters: $\mu_{11}$, $\mu_{10}$, $\mu_{00}$, $\mu_{01}$, $\delta_{00}$, $\delta_{10}$, $\delta_{01}$, $\delta_{11}$.
Initialize code parameters: code rate $R_c$, code length $L$, replication fact $\Pi_p$, the step $\Delta_s$, target cost $T_{cost}$. $\lambda = (\lambda_2, \lambda_3, \cdots, \lambda_{V_{max}})$ and $\rho = (\rho_2, \rho_3, \cdots, \rho_{C_{max}})$.
Calculate the MI of the quanzited LLR-value messages $I_{(\zeta,X)}$ and the corresponding variance $\delta_{mlc}^2$.
Optimize the degree sequence according to equation (5).
Obtain the protograph base matrix $H_B$ $(L_{pm} \times L_{pn})$ based on the slightly modified degree sequence, according to the initialization parameters.
Permute the edges of the nodes in the $\Pi_p$ replicas of the base protograph matrix $H_B$:
for $i = 1$ to $L_{pn}$ do
  for $j = 1$ to $\Pi_p$ do
    if (j == 1) then
      Select the check nodes with larger local girth based on the modified PEG algorithm.
    else
      for $l = 1$ to $N_i^d$ do
        // $N_i^d$ is the number of connections of the check nodes connected with the variable nodes $v_i$ of base matrix.
        $L_j^l = \frac{L_{j-1}^l}{J} \times \Pi_p + \left(L_{j-1}^l + 1\right) \mod \Pi_p$
      end for
    end if
  end for
end for
```

B. Asymptotic Ensemble Weight Distribution

The asymptotic ensemble weight distribution is employed to elaborate whether or not the code ensemble minimum distance grows linearly with the code length L. In this paper, we briefly review the computation method of the asymptotic ensemble weight distribution for the protograph based LDPC code[12]. Let τ_v and τ_c be the number of the variable node and check node for the photograph, respectively. Given the scalar normalized total codeword weight ζ, we define the code ensemble's normalized logarithmic asymptotic weight distribution as $\vartheta(\zeta)$, which are both normalized by the code length L. Accordingly, the normalized logarithmic asymptotic weight distribution for each vector $\boldsymbol{\zeta}$ of partial weights is define as

$$\vartheta(\boldsymbol{\zeta}) = \sum_{j=1}^{\tau_c} a^c(\boldsymbol{\zeta}_j) - \sum_{i=1}^{\tau_v}(d_v^i - 1)H_b(\zeta_i) \tag{6}$$

where $a^c(\boldsymbol{\zeta}_j)$ is a normalized logarithmic asymptotic weight distribution for check node c_j with normalized partial weight vector $\boldsymbol{\zeta}_j$, $H_b(\cdot)$ is the binary entropy function. Then, we can evaluate the normalized logarithmic asymptotic weight distribution $\vartheta(\zeta)$ for the protograph code ensemble as

$$\tau_v\vartheta(\zeta) = \max_{\boldsymbol{\zeta}:|\boldsymbol{\zeta_v}|=\tau_v\zeta}\vartheta(\boldsymbol{\zeta}) = \max_{\boldsymbol{\zeta_v}:|\boldsymbol{\zeta_v}|=\tau_v\zeta}\vartheta_v(\boldsymbol{\zeta_v}) \tag{7}$$

where $\vartheta_v(\boldsymbol{\zeta_v})$ for any subvector $\boldsymbol{\zeta_v}$ of normalized partial weights of the variable nodes is obtained by an unconstrained maximization of $\vartheta(\boldsymbol{\zeta})$ over the remaining components of $\boldsymbol{\zeta}$.

Let $\zeta = \zeta_{min}$ be the typical minimum distance ratio if that is the first zero crossing and $\vartheta(\zeta)$ is negative before zero crossing.

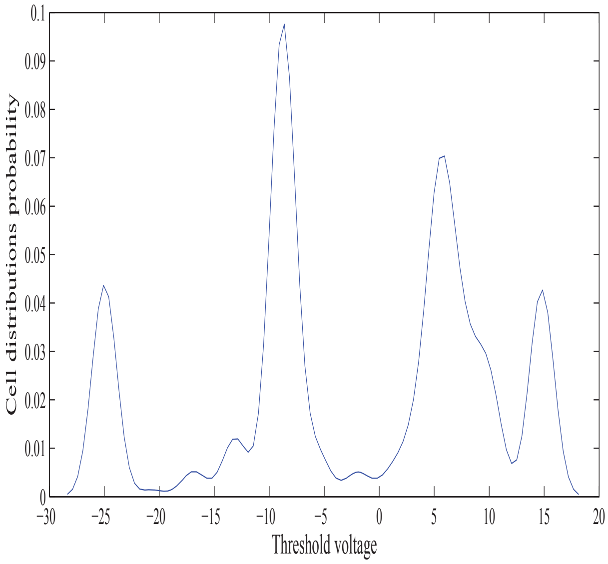
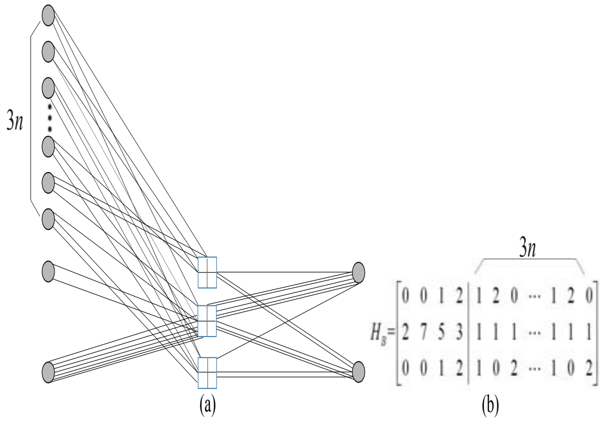


Fig. 2. The LLR distributions of readback signal voltage.



$$H_B=\left[\begin{array}{cccc|ccccccc} 0 & 0 & 1 & 2 & 1 & 2 & 0 & \cdots & 1 & 2 & 0 \\ 2 & 7 & 5 & 3 & 1 & 1 & 1 & \cdots & 1 & 1 & 1 \\ 0 & 0 & 1 & 2 & 1 & 0 & 2 & \cdots & 1 & 0 & 2 \end{array}\right]$$

Fig. 3. (a) Protograph of the proposed code. (b) Equivalent base matrix.

Then equation (7) can be applied to evaluate the ζ_{min} of the LDPC code ensemble built from the specific protograph.

IV. SIMULATION RESULTS

Simulation results are presented to evaluate the BER performance of the proposed coding schemes in a MLC NAND flash memory channel. In the simulations, we set the maximum number of BP iterations in LDPC decoder to 50, and all codes have rate of 0.8095. Also, a 3 bit-level quantizer is used. For the MLC channel, $v_{\max} = \mu_{01} - \mu_{11} = 6.5V$, δ is the standard deviation of the two inner distributions as shown in Fig.1.

The protograph and equivalent base matrix H_B of the proposed LDPC code based on the Algorithm 1 are give in Fig.3, where $n = 4$. Fig.4 depicts the asymptotic weight distributions and zero crossings for the proposed protograph LDPC code. We can see that the typical minimum distance ratio of the proposed photograph code $\zeta_{min} = 0.026$, which guarantees that the minimum distance of the LDPC code designed from the corresponding protograph grows linearly with block length N with proportionality ζ_{min}. The ζ_{min} can be further increased by reducing the proportion of degree-2 variable nodes in the protograph as shown in Fig.3 due to the fact that degree-2 variable nodes will introduce an error floor.

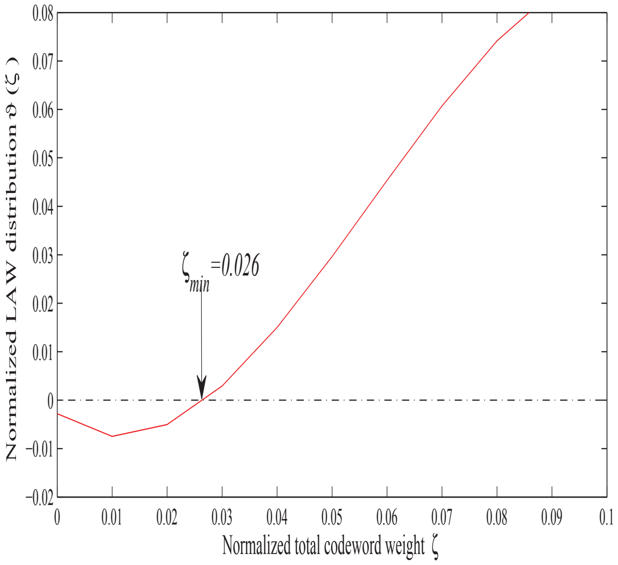


Fig. 4. Asymptotic weight distributions and zero crossings for the proposed Protograph LDPC code.

Note that the proposed nested photograph can also be employed to design the high rate-compatible LDPC codes with code rate $R_c = (3n+1)/(3n+4)$ by repeating the same nested sub-graph in Fig.3.

In Fig.5, we compare the BER performance of our proposed protograph codes (Scheme 1: QC-structure and random-structure) with the optimized random LDPC code (Scheme 2) and EG-QC LDPC code (Scheme 3) [13] for the same code length in the specific MLC NAND flash memory channel, where the base matrix of the proposed protograph LDPC codes is based on the Algorithm 1. Observe that the proposed Scheme 1 can provide gains of 0.7 dB over Scheme 3 at a BER of 10^{-6}. It can also be seen that the proposed protograph based QC-LDPC code in Scheme 1 yields similar BER performance compared to the random-structure protograph code and the significantly more complex, unstructured optimized codes at BER of 10^{-6}.

We also plot the frame error rate (FER) of the three schemes for comparison in Fig.6, where the frame size is the code length $L = 4032$. Fig.6 shows that our designed protograph LDPC codes for the specific MLC NAND flash memory channel can achieve better performance than the EG-QC LDPC codes while maintaining the low hardware storage space, which coincides with the results in Fig.5.

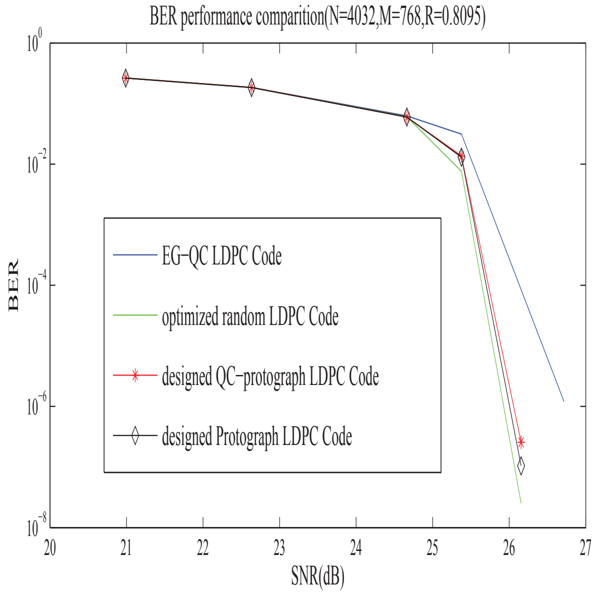


Fig. 5. BER performance comparison with different schemes in a MLC NAND flash memory channel.

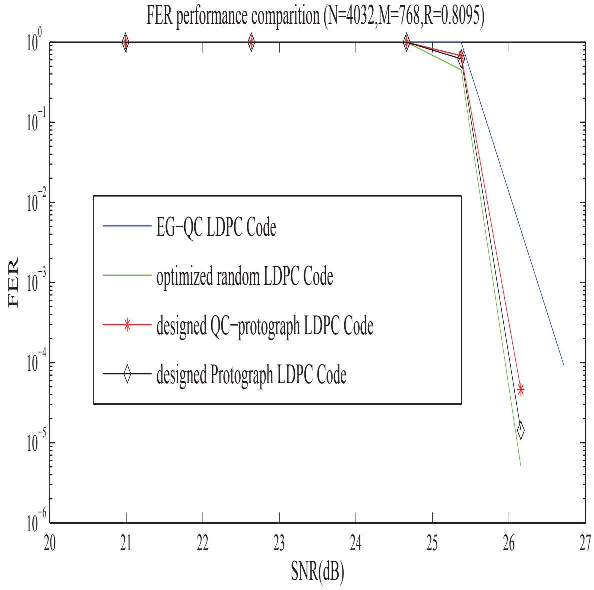


Fig. 6. FER performance comparison with different schemes in a MLC NAND flash memory channel.

V. CONCLUSION

New protograph based QC-LDPC codes have been proposed for MLC NAND flash channels. The proposed principles can be easily extended to other flash memory channels, and effectively used to design nested families of protograph LDPC codes. Monte Carlo simulation results have verified that our proposed protograph based QC-LDPC codes can perform very close to the unstructured optimized random LDPC codes, and achieve better performance than the EG-QC LDPC codes. We also have evaluated the performance of the proposed protograph LDPC codes by means of the asymptotic weight enumerator analysis. Hence the proposed approach provides a significant simplification for the MLC NAND flash system, since both the LDPC encoding and decoding complexity have been drastically reduced due to the protograph based QC structure.

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